What Is Claimed Is:

1. An apparatus that selectively multiplexes a plurality of signal lines through an I/O pin on a semiconductor chip, comprising:

the semiconductor chip;

the I/O pin on the semiconductor chip, for coupling a signal line within the semiconductor chip to a signal line outside of the semiconductor chip;

a transmitting circuit that is configured to selectively multiplex the plurality of signal lines onto the I/O pin;

a receiving circuit that is configured to receive multiplexed data from the I/O pin, and to reverse the multiplexing so that values originally from the multiplexed signal lines are separated into distinct signals in the receiving circuit;

wherein the transmitting circuit and the receiving circuit are driven by a common clock signal coupled to both the transmitting circuit and the receiving circuit; and

an initialization circuit, coupled to the transmitting circuit and the receiving circuit, that selectively configures the transmitting circuit and the receiving circuit to multiplex at least one of the plurality of signal lines through the I/O pin.

2. The apparatus of claim 1, further comprising a synchronizing circuit, coupled to the transmitting circuit and the receiving circuit that synchronizes the transmitting circuit and the receiving circuit by simultaneously sending a reset signal to both the transmitting circuit and the receiving circuit.

3. The apparatus of claim 1, wherein the transmitting circuit is located on the semiconductor chip and the receiving circuit is located off of the semiconductor chip.

4. The apparatus of claim 1, wherein the receiving circuit is located on the semiconductor chip and the transmitting circuit is located off of the semiconductor chip.

5. The apparatus of claim 1, wherein the semiconductor chip is a core logic chip that couples together a processor, a memory and a peripheral bus in a computer system.

6. The apparatus of claim 1, wherein the initialization circuit communicates information identifying the selected signal lines to both the transmitting circuit and the receiving circuit.

7. The apparatus of claim 1, wherein the initialization circuit is located on the semiconductor chip.

8. The apparatus of claim 1, wherein the initialization circuit is located externally to the semiconductor chip.

9. The apparatus of claim 1, wherein the I/O pin is bi-directional, and further comprising a second transmitting circuit and a second receiving circuit for communicating through the I/O pin in a reverse direction.

10. The apparatus of claim 1, wherein the initialization circuit is configured to initialize the transmitting circuit and the receiving circuit during a computer system boot up operation.

11. The apparatus of claim 1, wherein the receiving circuit includes:

a plurality of memory elements coupled to the I/O pin for storing data values received from the I/O pin; and

a control circuit that selectively enables the plurality of memory elements so as to record data values from signal lines in corresponding memory elements.

12. The apparatus of claim 1, wherein the transmitting circuit includes:

a multiplexer for multiplexing the plurality of signal lines onto the I/O pin; and

a control circuit that controls the multiplexer so that the at least one of the plurality of signal lines is multiplexed onto the I/O pin.

13. An apparatus that selectively multiplexes a plurality of signal lines through an I/O pin on a semiconductor chip, wherein the semiconductor chip is a core logic chip that couples together a processor, a memory and a peripheral bus in a computer system, the apparatus comprising:

the semiconductor chip;

the I/O pin on the semiconductor chip, for coupling a signal line within the semiconductor chip to a signal line outside of the semiconductor chip;

a transmitting circuit that is configured to selectively multiplex the plurality of signal lines onto the I/O pin;

a receiving circuit that is configured to receive multiplexed data from the I/O pin, and to reverse the multiplexing so the multiplexed data is separated into distinct signals in the receiving circuit;

wherein the transmitting circuit and the receiving circuit are driven by a common clock signal coupled to both the transmitting circuit and the receiving circuit;

an initialization circuit, coupled to the transmitting circuit and the receiving circuit, that selectively configures the transmitting circuit and the receiving circuit to multiplex at least one selected signal line from the plurality of signal lines through the I/O pin;

wherein the initialization circuit communicates information identifying the at least one selected signal line to both the transmitting circuit and the receiving circuit;

wherein the initialization circuit is configured to initialize the transmitting circuit and the receiving circuit during a computer system boot up operation; and

a synchronizing circuit, coupled to the transmitting circuit and the receiving circuit, that synchronizes the transmitting circuit and the receiving circuit by simultaneously sending a reset signal to both the transmitting circuit and the receiving circuit.

14. The apparatus of claim 13, wherein the receiving circuit includes:

a plurality of memory elements coupled to the I/O pin for storing data values received from the I/O pin; and

a control circuit that selectively enables the plurality of memory elements so as to record data values from the at least one selected signal line into corresponding memory elements.

15. The apparatus of claim 13, wherein the transmitting circuit includes:

a multiplexer for multiplexing the plurality of signal lines onto the I/O pin; and

a control circuit that controls the multiplexer so that the at least one selected signal line is multiplexed onto the I/O pin.

16. The apparatus of claim 13, wherein the receiving circuit is located on the semiconductor chip and the transmitting circuit is located off of the semiconductor chip.

17. The apparatus of claim 13, wherein the initialization circuit is located on the semiconductor chip.

18. The apparatus of claim 13, wherein the initialization circuit is located externally to the semiconductor chip.

19. An computer system that selectively multiplexes a plurality of signal lines through an I/O pin, comprising:

a processor;

a memory;

a semiconductor chip within the computer system containing circuitry for performing computer system operations;

the I/O pin on the semiconductor chip, for coupling a signal line within the semiconductor chip to a signal line outside of the semiconductor chip;

a transmitting circuit that is configured to selectively multiplex the plurality of signal lines onto the I/O pin;

a receiving circuit that is configured to receive multiplexed data from the I/O pin, and to reverse the multiplexing so that values originally from the multiplexed signal lines are separated into distinct signals in the receiving circuit;

wherein the transmitting circuit and the receiving circuit are driven by a common clock signal coupled to both the transmitting circuit and the receiving circuit; and

an initialization circuit, coupled to the transmitting circuit and the receiving circuit, that selectively configures the transmitting circuit and the receiving circuit to multiplex at least one of the plurality of signal lines through the I/O pin.

20. The computer system of claim 19, wherein the receiving circuit includes:

a plurality of memory elements coupled to the I/O pin for storing data values received from the I/O pin; and

a control circuit that selectively enables the plurality of memory elements so as to record data values from the at least one selected signal line into corresponding memory elements.

21. The computer system of claim 19, wherein the transmitting circuit includes:

a multiplexer for multiplexing the plurality of signal lines onto the I/O pin; and

a control circuit that controls the multiplexer so that the at least one selected signal line is multiplexed onto the I/O pin.